AND8481/D

A High−Efficiency, 300 W Bridgeless PFC Stage

Prepared by: Joël TURCHI
ON Semiconductor

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APPLICATION NOTE

Introduction

Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80plus initiative and moreover its bronze, silver and gold derivatives force desktops and servers manufacturers to work on innovative solutions. An important focus is on the PFC stage that with the EMI filter can consume 5% to 8% of the output power at low line, full load.

Bridgeless PFC is one of the options to meet these new requirements. In addition to general considerations, a precedent application note [1] presented the 2−phase bridgeless structure that was preferred to drive a 800 W, wide mains application.

Because of its merits (ease of implementation, EMI−friendly characteristics, high efficiency...) the 2−phase approach is re−used for a lower power application (300 W, wide mains). This paper presents the experimental performance obtained with this approach.

2−Phase Approach

This bridgeless solution detailed in [1], was proposed by Professors Alexandre Ferrari de Souza and Ivo Barbi ([2]). Comparison elements to other bridgeless structures can also be found in [3].

Figure 1 summarizes 2−phase approach functioning. There is no diodes bridge to rectify the line sine−wave. Only two diodes are implemented to attach the line terminal that is at the lowest potential to the application ground. More specifically, the solution can be viewed as a 2−phase PFC where the two branches operate in parallel:

- For the half−wave when the terminal “PH1” of the line is high, diode $\boldsymbol{D_1}$ is off and $\boldsymbol{D_2}$ connects the PFC ground to the negative line terminal (“PH2”). $\boldsymbol{D_2}$ grounds the input of the “PH2 PFC stage” branch that thus, is inactive and the “PH1 PFC stage” processes the power.
- For the second half−line cycle (when “PH2” is high), the “PH2 PFC stage” branch is operating and “PH1 PFC stage” that has no input voltage, is inactive.

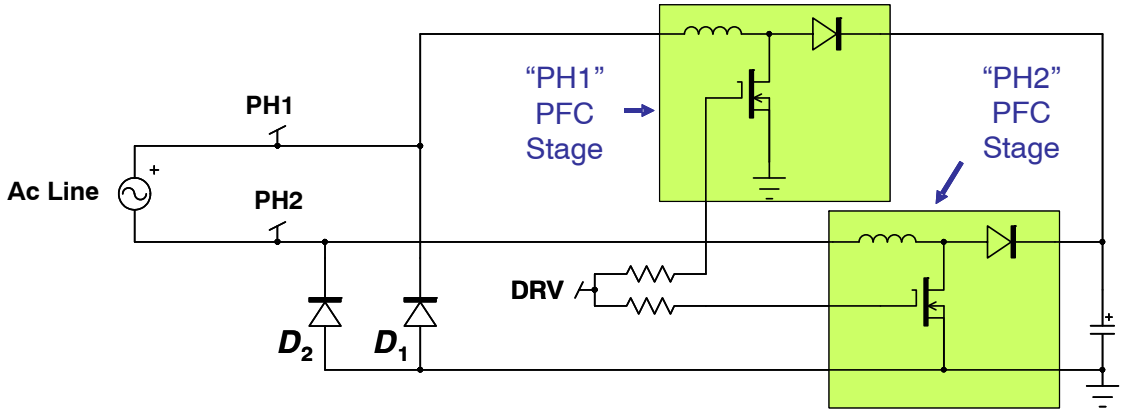


Figure 1. 2−Phase Architecture

One interesting characteristic of this structure is that the PFC stage that is active, behaves as a conventional PFC boost would do:

- When the “PH1” terminal is positive, diode $\boldsymbol{D_1}$ opens and $\boldsymbol{D_2}$ offers the return path. The input voltage for the “PH1” PFC stage is a rectified sinusoid referenced to ground.
- For the other half−wave when “PH2” is the positive terminal, $\boldsymbol{D_1}$ offers the return path. Diode $\boldsymbol{D_2}$ is off and sees a rectified sinusoid that inputs the “PH2” PFC stage. Again, we have a conventional PFC where the input voltage and the boost are traditionally referenced to ground.

It is also worth reminding that the 2−phase structure does not require any specific controller. The MOSFETs of the two branches are referenced to ground and they can be permanently driven even when their phase is in idle phase. Simply, the MOSFET of the inactive branch is then turned on and off useless.

As detailed in [1], the main inconvenience of this structure is that part of the input current does not flow through the supposed (D_1 or D_2) return path as it is diverted by the MOSFET body diode and inductor of the inactive branch. That is why current sense transformers can be of great help to measure the current in such a structure.

Implementation of the Bridgeless PFC

Figure 2 highlights the main parts of our 300 W prototype.

Diodes Bridge:

Amazingly, a diode bridge is implemented. However, it does not serve as a traditional input bridge to rectify the line (as shown by Figure 2, the two branches are directly connected to the line terminals). Here, the upper diodes (D_3 and D_4) play the role of the bypass diode that in a conventional PFC, diverts the in−rush current taking place when the PFC stage is plugged in (Note 1). Unless an overload situation occurs, these diodes are off for the rest of time.

The bottom diodes (D_1 and D_2) have the function that was described in the precedent section.

Input Voltage Sensing:

The NCP1605 monitors the input voltage for brown−out detection. Two small axial diodes (e.g., 1N4007) rectify the line voltage to obtain a rectified sinusoid that is then scaled down and filtered to sense a voltage proportional to the line voltage.

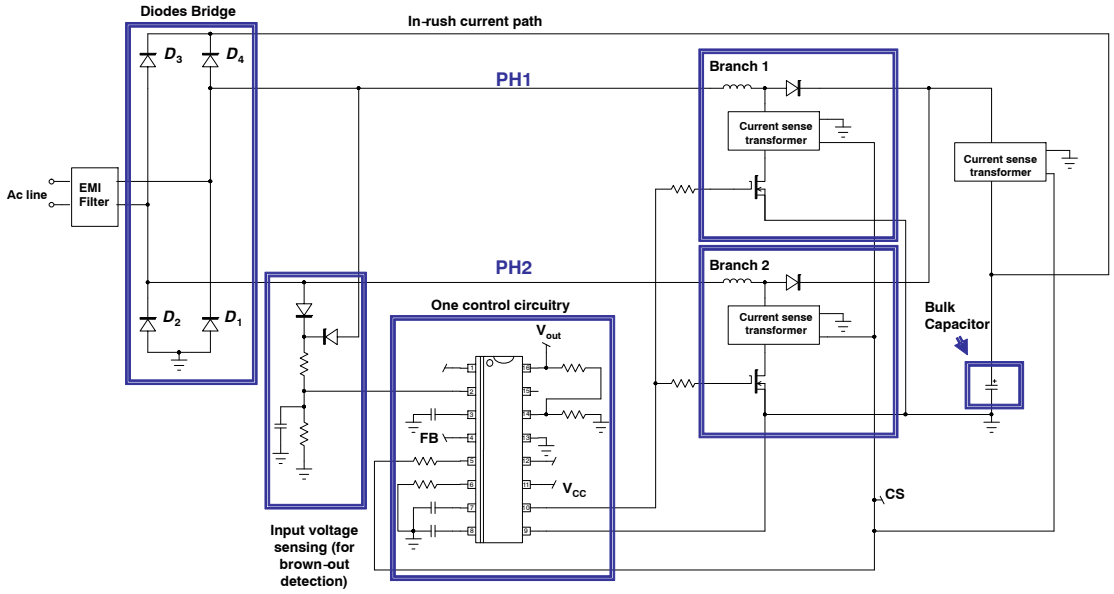


Figure 2. Simplified Application Schematic

1. As in a conventional PFC boost, there is no switch between the line and the bulk capacitor able to prevent the line from directly charge the bulk capacitor. That is why an in−rush takes place that charges the bulk capacitor to the line peak voltage. This in−rush current can be huge if not limited by some dedicated circuitry. D_3 (D_4) conducts the in−rush current when the terminal “PH2” (“PH1”) is at the highest level.

Branch 1 and Branch 2 of the PFC Boost:

Two (identical) PFC boost converters are to be designed. This application note does not focus on the dimensioning of the power components since it is relatively traditional. However, the fact that each branch is active for one half−line cycle only, improves the heating distribution. Also, the rms current being halved in each branch, the power components does not need to be as large as those of a conventional PFC.

Control Circuitry:

The 800 W application of [1] runs in Continuous Conduction Mode (CCM) as this operating mode is appropriate for this power range. For the 300 W, CCM can still be used but ***F***requency ***C***lamped ***Cr***itical conduction ***M***ode (FCCrM) has proven to be a particularly efficient solution for this power level or below.

FCCrM is a technique embedded in controllers like the NCP1605 or the NCP1631 from ON Semiconductor ([4] and [5]). When operated in this mode, ***P***ower ***F***actor ***C***orrection (*PFC*) stages run in Critical conduction Mode (CrM) in heavy load conditions but limit the switching frequency that otherwise would "take off" in medium/light load conditions (Note 2). As shown in [6], FCCrM allows for the use of smaller inductors compared to those required by traditional CrM circuits.

FCCrM controllers do not only limit the frequency. Clamping the frequency of a CrM circuit dramatically affects the power factor. That is why FCCrM controllers also modulate the on−time in DCM operation in order to continue properly shaping the input current. More specifically, they permanently monitor the dead−time relative duration over each switching period and as a function of this information, adjust the on−time ([4] and [5]). Doing so, FCCrM PFC stages still exhibit near−unity power factor even if the switching frequency is clamped. More generally, they transition from CrM to DCM and vice versa without discontinuity in the power transfer and without power factor degradation.

The NCP1605 FCCrM controller was then selected to drive the application. Housed in a SOIC16 package, the circuit incorporates all the features necessary for building robust and compact PFC stages, with a minimum of external components. It also features a high−voltage current source to pre−charge the V_{CC} capacitor, a dynamic response enhancer and a "pfcOK" signal to enable/disable the downstream converter. These functions ease and optimize the design of resonant or forward converters that would load the PFC stage, since such power supplies take benefit of a narrow input voltage range. In addition, the NCP1605 integrates the skip cycle capability to lower the stand−by losses to a minimum.

Current Sense Circuitry:

As aforementioned and further detailed in [1], a portion of the input current does not flow through the supposed return path but is diverted by the MOSFET body diode and the inductor of the inactive branch. Thus, inserting a current sensing resistor in the supposed return path is not a satisfactory option to monitor the current. Instead, current sense transformers (CTs) can provide an efficient solution.

The input current is absorbed by L_1 for one half−line cycle and by L_2 for the other one. Unfortunately, it is impossible to directly monitor the current in these components by the means of CTs since they convey a continuous current. Instead, the MOSFETs and diode currents are sensed. Since these components are off part of the switching period, they allow the cycle−by−cycle CTs demagnetization.

As shown in Figure 3, three CTs are placed to sense the total input current:

- CT_1 and CT_2 monitor the current flowing through the MOSFETs
- CT_3 monitors the total current provided by the two boost diodes

2. FCCrM controller modulates the duty−ratio so that the line current keeps properly shaped even when the frequency is clamped.

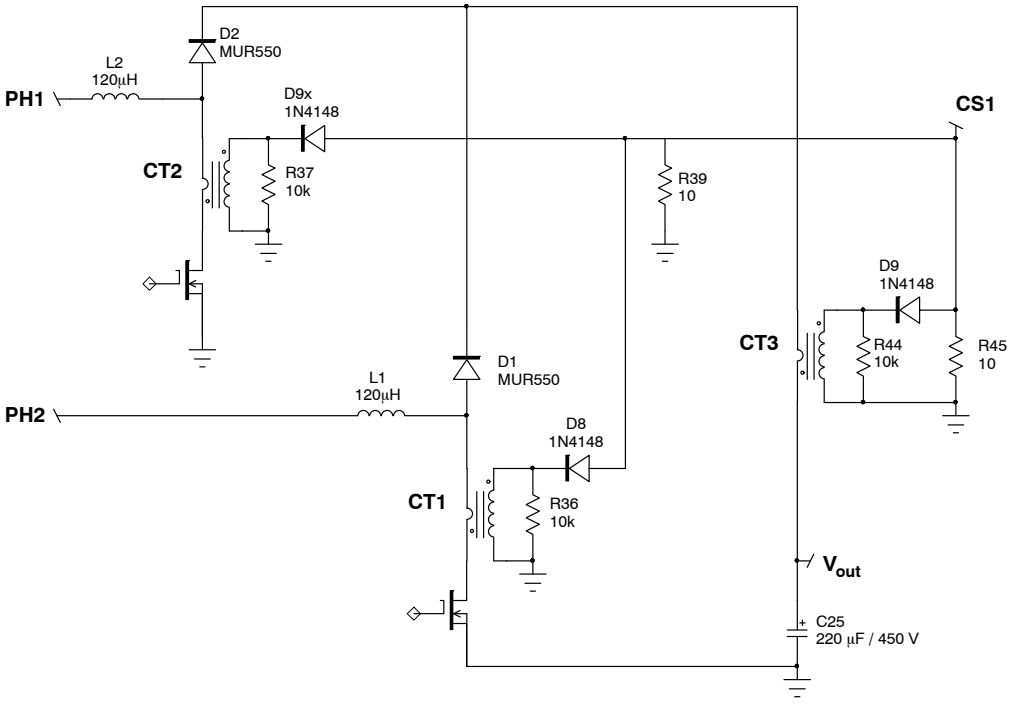


Figure 3. Current Sense Circuitry

They all are identically configured. A 10 kΩ resistor is placed across the secondary winding to reset the core when no current flows into the primary side. A diode is placed that separates the demagnetization current from the useful signal. The three diodes are all connected together so that the *CS*1 common node receives a current proportional to the total input current. This current is collected by resistor (R_{CS} = R_{39} // R_{45}) (see Figure 3) to generate the following voltage:

$$V_{RCS} = -\frac{N_p}{N_s} \cdot R_{CS} \cdot I_{in} \qquad \text{(eq. 1)}$$

The obtained voltage is negative. This is because the NCP1605 is a negative−sensing circuit (its current sense pin is designed to monitor a negative voltage proportional to the input current). This is why the CTs are implemented in such a way that the non−grounded terminal of the secondary winding draws a current for the monitoring phase when the primary side sees the current under interest. The diode is coupled to allow the current circulation during the monitoring phase.

As a matter of fact, this is like if the current was sensed through a current sense resistor R_{SENSE} equating:

$$\left(R_{SENSE} = \frac{N_p}{N_s} \cdot R_{CS}\right)$$

In our case,

$$\left(\frac{N_p}{N_s} = \frac{1}{50}\right)$$

and (R_{39} = R_{45} = 10 Ω) leading to: (R_{SENSE} ≅ 100 mΩ).

R_{CS} is split into two paralleled 10 Ω resistors to ease the board lay−out and improve the current sensing noise immunity.

Application Schematic:

Figure 4 shows the application schematic. The controller is supplied by a 15 V dc external power source (V_{aux}). The NCP1605 latch−off pin is used to disable the circuit if V_{CC} exceeds 17.5 V (level controlled by components D_7, R_{32}, R_{33}).

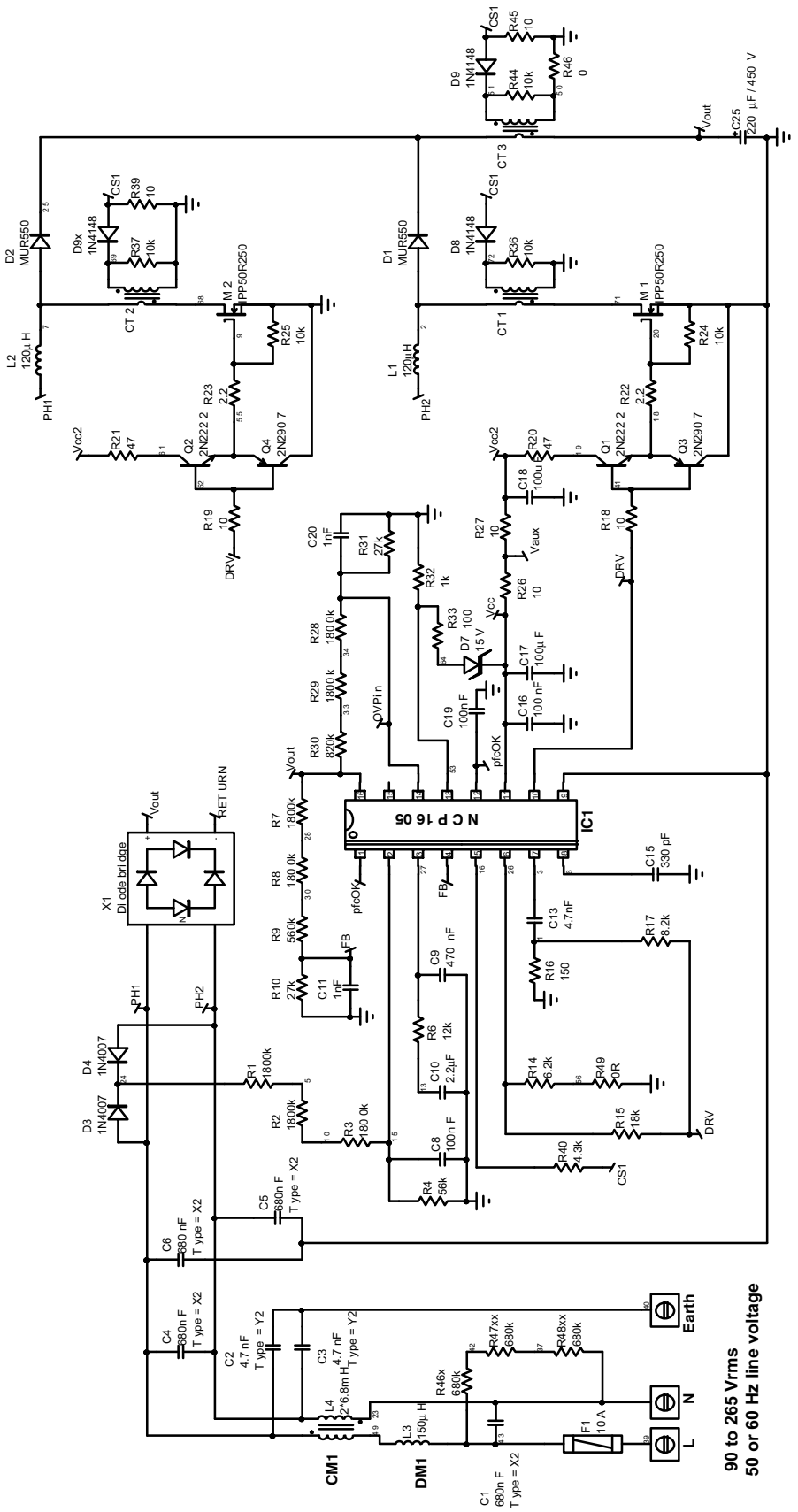


Figure 4. Application Schematic

Main Components of the Board:

Figure 5 shows the prototype. It consists of the main following components:

- Diodes Bridge: KBU6K from General Semiconductor (6 A, 800 V)
- Current sense transformers (1 per branch, a third one to sense the total current provided by the boost diodes): WCM601−2 from West Coast Magnetics (20 A, 50 turns)
- Boost diodes (1 per branch): MUR550 (5−A, 520−V DCM PFC Specific Ultrafast) from ON Semiconductor
- Power MOSFETs (1 per branch): IPP50R250 from Infineon (550 V, 250 mΩ, 27 nC) or IPP60R099 from Infineon (650 V, 99 mΩ, 60 nC)
- Inductors (1 per branch): 115 μH / 10 A_{pk} inductor (PQ32/20) provided by CME
- Controller: NCP1605 from ON Semiconductor

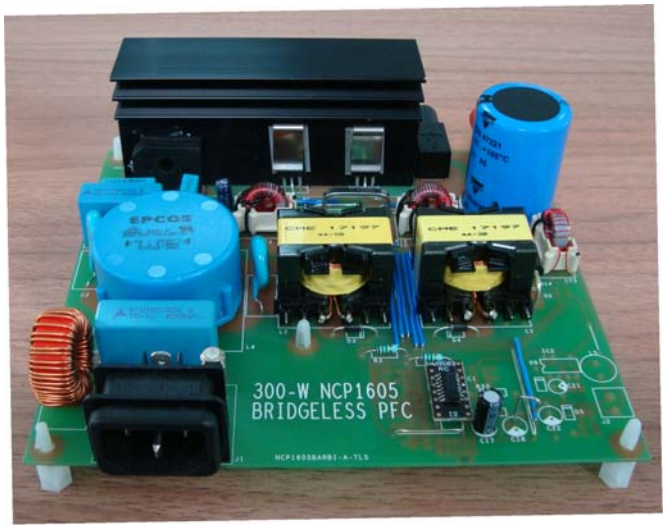
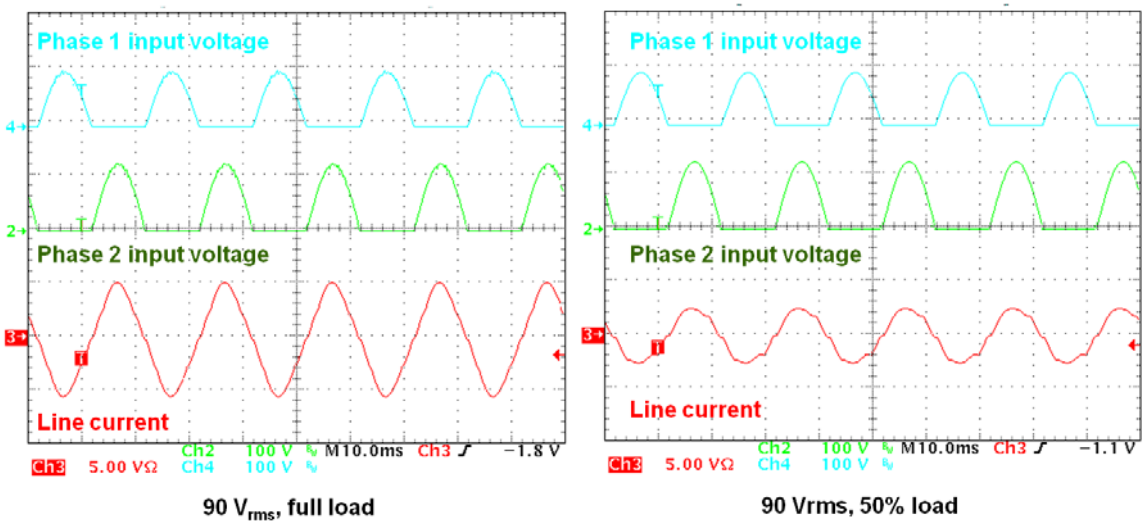


Figure 5. Photograph of the Prototype

Performance of the 300 W board

Typical Waveforms



90 V_{rms}, full load

90 Vrms, 50% load

Figure 6. Typical Waveforms at Low Line and 100% (Left) and 50% of the Load (Right)

Plots of Figure 6 were obtained at the lowest line level (90 V_{rms}). They portray the typical waveforms at full and mid−load. As expected, the input voltage of the “PH1 PFC stage” is a rectified sinusoid for one half−line cycle and null for the other one. The input voltage of the “PH2 PFC stage” behaves the same but in an out−of−phase manner.

The line current is properly shaped.

Thermal measurements

The following results were obtained using a thermal camera, after a 1/2 h operation. The board was operating at a 25°C ambient temperature, without a fan. These data are indicative.

For the bridge, the MOSFETs and diodes, the measures were actually made on the heat−sink as near as possible of the components of interest.

Measurement conditions:

$V_{in,rms}$ = 90 V
P_{out} = 300 W
PF = 0.996
THD = 8%

Devices	EMI CM Choke	EMI DM Choke	Input Bridge	M1	M2	Bulk Capacitor	L1	L2	D1	D2	NCP1605
Temp (°C)	62	47	60	75	65	40	67	68	69	63	43

Total Harmonic Distortion (THD)

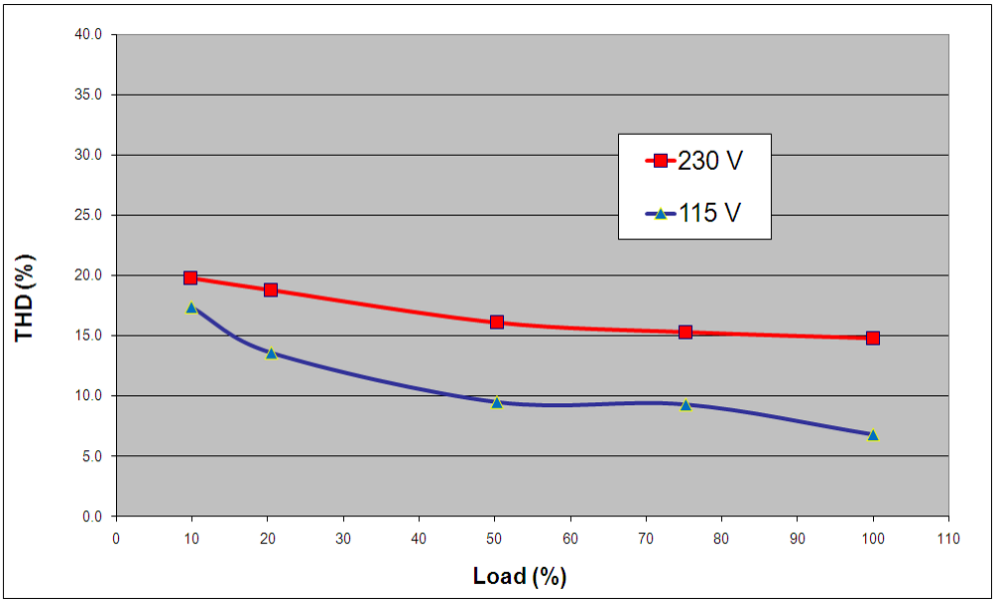


Figure 7. THD Versus Load @ 115 and 230 V_{rms}

Figure 7 shows the THD performance as a function of the load at two different line rms voltages: 115 and 230 V. One can note that the total harmonic distortion remains very low over the whole range (from 10% to 100% of the load). In particular, THD still remains below 20% at 230 V and 10% of the load where the line current is small and more sensitive to all the sources of distortion like those caused by the EMI filter.

Efficiency

Figures 8 to 10 portray the efficiency over the line range, from 10% to 100% of the load at three different line magnitudes (90, 115 and 230 V).

The efficiency has been measured with two different MOSFETs from Infineon:

- IPP50R250 (TO220, 550 V, 250 mΩ, 27 nC)
- IPP60R099 (TO220, 650 V, 99 mΩ, 60 nC)

The PFC stage was tested in the following conditions:

Open frame, 25°C ambient temperature, no fan

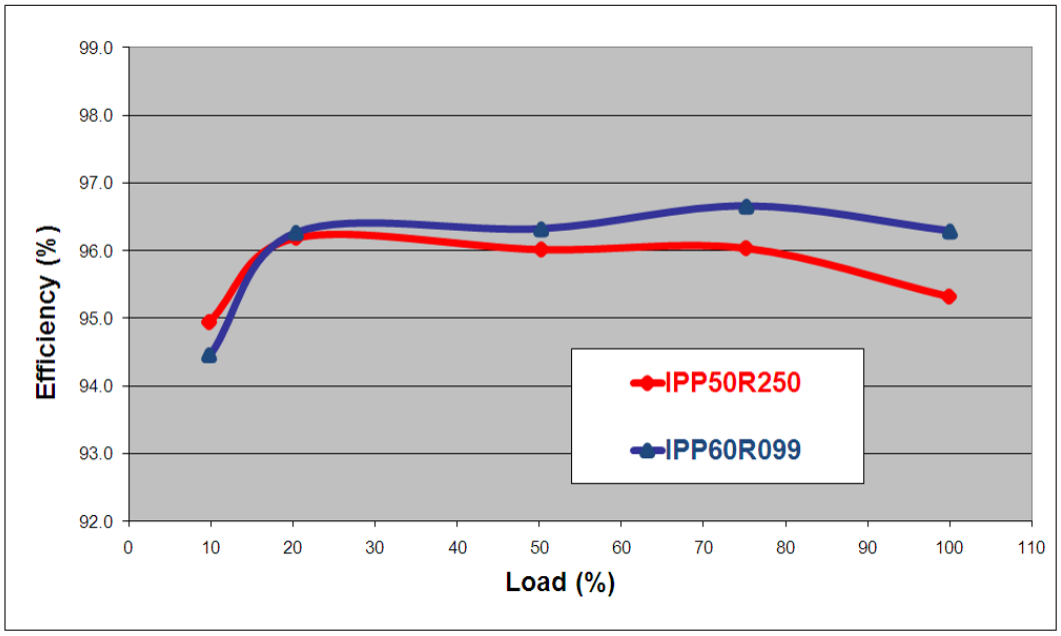


Figure 8. Efficiency Performance @ 90 V_{rms} with Two Different MOSFETs

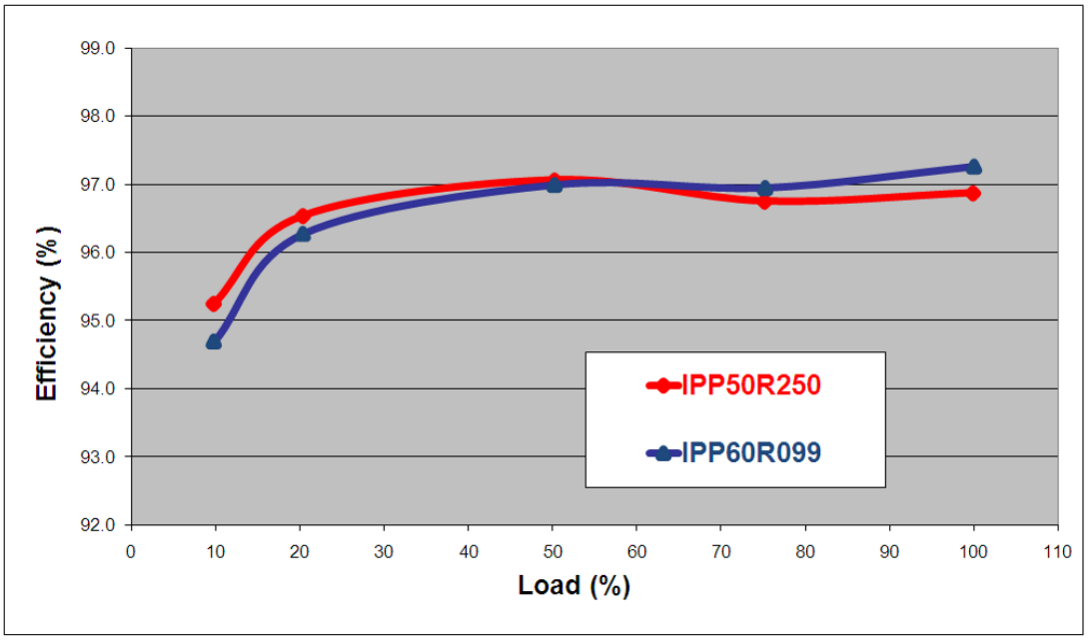


Figure 9. Efficiency Performance @ 115 V_{rms} with Two Different MOSFETs

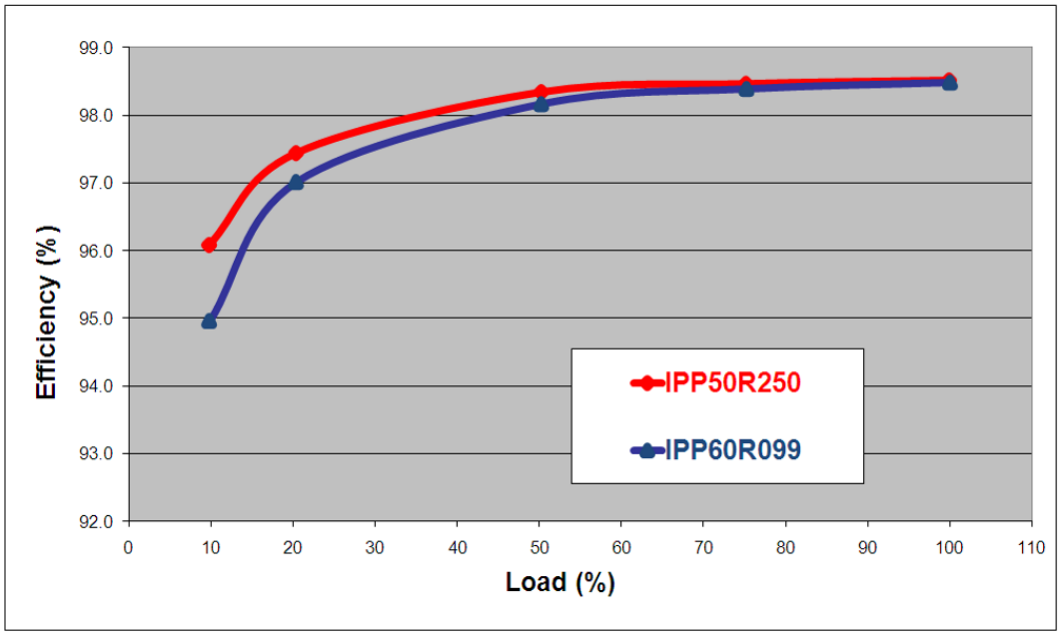


Figure 10. Efficiency Performance @ 230 V_{rms} with Two Different MOSFETs

In the light of Figures 8 to 10, we can note that:

- Like in a conventional PFC, the efficiency is much higher at high line.
- At the lowest line level (90 V_{rms}), the efficiency firmly remains higher than 96% from 20% to 100% of the load with the lowest $R_{DS(on)}$ MOSFET (IPP60R099). When the IPP50R250 is used, the conduction losses are higher. The full load efficiency drops to 95.3%.
- At low line (115 V_{rms}), the full−load efficiency is improved since the conduction losses are lower. The reduced impact of the conduction losses also explain that the performance are less dependent on the selected MOSFET
- At high line (230 V_{rms}), the efficiency exceeds 97% from 20% to 100% of the load with the two MOSFETs.
- At 10% of the load, the efficiency is worse with the lowest $R_{DS(on)}$ MOSFET (IPP60R099) in the three line cases under consideration. This is because the switching losses are increased with this component (higher gate charge and parasitic capacitors). However, it remains high in all cases (in the range of 95% or more at 115 and 230 V) as ***the frequency clamp contains the switching losses***.
- The light−load efficiency could have been further improved if the standby management featured by the NCP1605 (soft−skip mode) had been enabled. Soft−skip is normally driven by the downstream converter (by its feedback for instance). As the board only consists of the PFC stage, this function was here disabled. Some circuitry could also be added to reduce the clamp frequency in light load conditions.

Conclusion

A bridgeless PFC based on the 2−phase architecture has several merits among which one can list the ease of control or the absence of high−frequency noise injected to the line (eased EMI).

The paper presents the performance of a wide−mains, 300 W prototype controlled by the NCP1605 in so called Frequency Clamped Critical conduction Mode (FCCrM).

The prototype has been tested without a fan (open frame, 25°C ambient temperature). In these conditions, the 20% to 100% load efficiency was measured as higher than 96% at low line and greater than 97% at high line. The THD remains very low.

More details can be found in [7] that further compares the performance of this prototype to those of an interleaved PFC.

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7. Joel Turchi, “Bridgeless and interleaved PFC stages for high efficiency − Comparison in a wide−mains, 300 W application”, PCIM 2010

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